## **DISCRETE SEMICONDUCTORS**

# DATA SHEET

**PEMD6**; **PUMD6** NPN/PNP resistor-equipped transistors; R1 =  $4.7 \text{ k}\Omega$ , R2 = open

Product specification Supersedes data of 2003 Nov 04 2004 Apr 07





# NPN/PNP resistor-equipped transistors; R1 = 4.7 k $\Omega$ , R2 = open

## PEMD6; PUMD6

#### **FEATURES**

- Built-in bias resistors
- · Simplified circuit design
- Reduction of component count
- · Reduced pick and place costs.

#### **APPLICATIONS**

- · Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- · Control of IC inputs.

#### **DESCRIPTION**

NPN/PNP resistor-equipped transistors (see "\_Data\_Sheet\_Remark Supersedes data of 2003 Nov 04" for package details).

#### **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	_	50	V
Io	output current (DC)	_	100	mA
TR1	NPN	_	_	_
TR2	PNP	_	_	_
R1	bias resistor	4.7	_	kΩ
R2	open	_	_	_

#### **PRODUCT OVERVIEW**

TYPE NUMBER	PACH	(AGE	MARKING CODE	NPN/NPN PNP/PN		
I TPE NOWBER	PHILIPS	EIAJ	MARKING CODE	COMPLEMENT	COMPLEMENT	
PEMD6	SOT666	_	D6	PEMH7	PEMB3	
PUMD6	SOT363	SC-88	D*6 <sup>(1)</sup>	PUMH7	PUMB3	

#### Note

- 1. \* = p: Made in Hong Kong.
  - \* = t: Made in Malaysia.

#### SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING		
I TPE NUMBER	SIMPLIFIED OUTLINE AND STMBOL	PIN	DESCRIPTION	
PEMD6; PUMD6	6 5 4	1	emitter TR1	
		2	base TR1	
	R1	3	collector TR2	
	TR2	4	emitter TR2	
		5	base TR2	
		6	collector TR1	
	Top view мнсо28			

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#### **ORDERING INFORMATION**

TYPE	PACKAGE				
NUMBER	NAME DESCRIPTION VER				
PEMD6	_	plastic surface mounted package; 6 leads	SOT666		
PUMD6	_	plastic surface mounted package; 6 leads			

#### **LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT			
Per transistor; for the PNP transistor with negative polarity								
V <sub>CBO</sub>	collector-base voltage	open emitter	-	50	V			
V <sub>CEO</sub>	collector-emitter voltage	open base	_	50	V			
V <sub>EBO</sub>	emitter-base voltage	open collector	_	5	V			
Io	output current (DC)		_	100	mA			
I <sub>CM</sub>	peak collector current		_	100	mA			
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1						
	SOT363	note 1	_	200	mW			
	SOT666	notes 1 and 2	-	200	mW			
T <sub>stg</sub>	storage temperature		-65	+150	°C			
Tj	junction temperature		_	150	°C			
T <sub>amb</sub>	operating ambient temperature		-65	+150	°C			
Per device					•			
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1						
	SOT363	note 1	-	300	mW			
	SOT666	notes 1 and 2	_	300	mW			

#### **Notes**

- 1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
- 2. Reflow soldering is the only recommended soldering method.

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#### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transis	stor			
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient SOT363 SOT666	note 1	625 625	K/W K/W
Per device	•			
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient SOT363	note 1	416	K/W
	SOT666		416	K/W

#### Note

## **CHARACTERISTICS**

 $T_{amb}$  = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Per transis	Per transistor; for the PNP transistor with negative polarity							
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	_	_	100	nA		
I <sub>CEO</sub>	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_{B} = 0$	_	_	1	μΑ		
		$V_{CE} = 30 \text{ V}; I_{B} = 0; T_{j} = 150 ^{\circ}\text{C}$	_	_	50	μΑ		
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	_	_	100	nA		
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 1 mA	200	_	_			
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}$	_	_	100	mV		
R1	input resistor		3.3	4.7	6.1	kΩ		
C <sub>c</sub>	collector capacitance	$I_E = I_e = 0$ ; $V_{CB} = 10 \text{ V}$ ; $f = 1 \text{ MHz}$						
	TR1 (NPN)		-	-	2.5	pF		
	TR2 (PNP)		_	_	3	pF		

<sup>1.</sup> Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

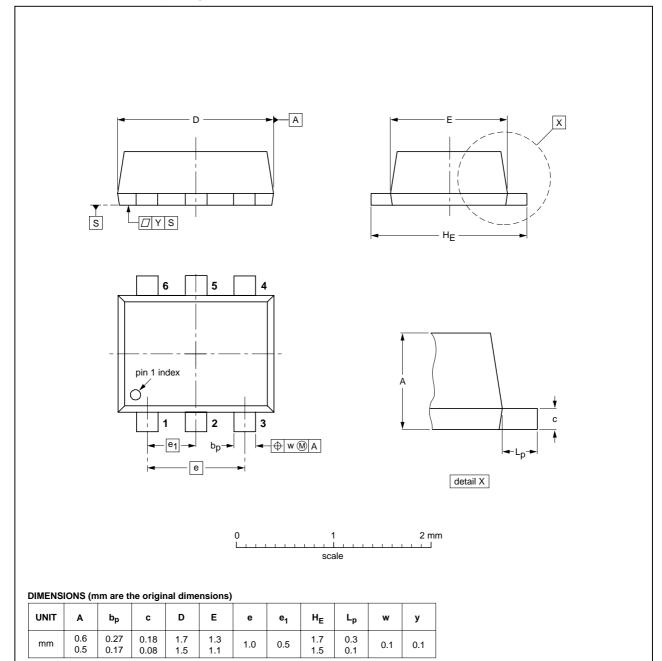
# NPN/PNP resistor-equipped transistors; R1 = 4.7 k $\Omega$ , R2 = open

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#### **PACKAGE OUTLINES**

### Plastic surface mounted package; 6 leads

SOT666



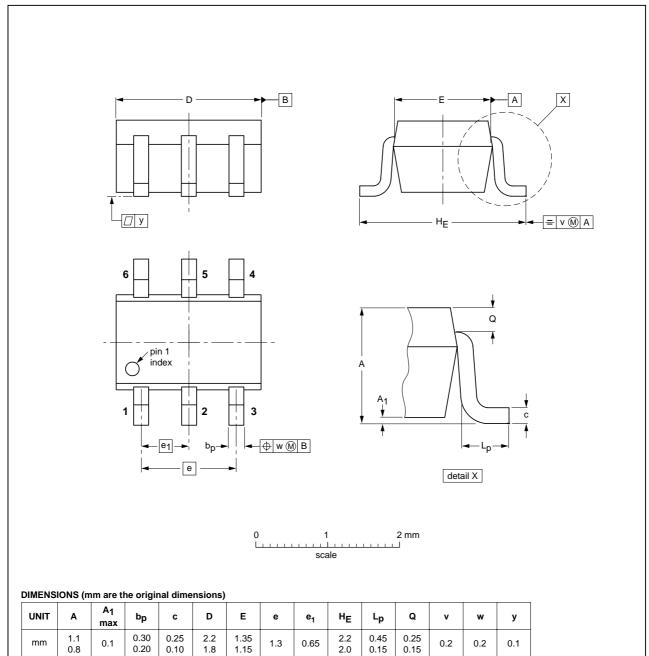
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# NPN/PNP resistor-equipped transistors; $R1 = 4.7 \text{ k}\Omega$ , R2 = open

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### Plastic surface mounted package; 6 leads

**SOT363** 



OUTLINE		REFERENCES				ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT363			SC-88			97-02-28	

0.45

0.25

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0.25

0.20

2.2

## NPN/PNP resistor-equipped transistors; R1 = 4.7 k $\Omega$ , R2 = open

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#### **DATA SHEET STATUS**

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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